



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,460	09/10/2003	Myounggoo Lee	101136-00095	2221

7590 02/05/2007  
ARENT FOX KINTNER PLOTKIN & KAHN, PLLC  
Suite 400  
1050 Connecticut Avenue, N.W.  
Washington, DC 20036-5339

EXAMINER
----------

MCDONALD, RODNEY GLENN

ART UNIT	PAPER NUMBER
----------	--------------

1753

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/05/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

## Office Action Summary

Application No.

10/658,460

Applicant(s)

LEE ET AL.

Examiner

Rodney G. McDonald

Art Unit

1753

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 16 November 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-3, 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gopalraja et al. (U.S. Pat. 6,193,855) in view of Shimamura et al. (U.S. Pat. 4,963,239).

For claim 1, Applicant requires a bias sputtering film forming process for forming a thin film by applying both voltages of a cathode voltage and a substrate bias voltage, wherein a thin film is formed on a substrate whereon an irregularity is formed in the state wherein only the cathode voltage out of said both voltages applied, and sputtering film forming is performed while continuously varying said substrate bias voltage so that

Art Unit: 1753

the thickness of said thin film formed on the surfaces on the sidewalls and on the bottoms of said irregularity is substantially uniform, wherein said substrate bias voltage corresponds to a stored value in a database stored in a control system.

For claim 3, Applicant requires the sputtering particles to be substantially vertically entering the substrate.

For claim 5, Applicant requires a bias sputtering film forming apparatus comprising an AC power source of a DC power source of variable output against substrate electrodes and a control system wherein the control system makes the cathode voltage set to a predetermined voltage previously, stores the substrate bias voltage value when the substrate is apart from the target by a predetermined distance and the thickness distribution of thin films on each of said surfaces corresponding to said substrate bias voltage value as reference data, and controls the output of said power source such that it is continuously varied based on bias voltage functions produced by selecting the substrate bias voltage value from the database, that makes said film thickness substantially uniform from said reference data when each of said surfaces is formed.

For claim 2, Applicant requires the cathode voltage to be varied while varying the substrate bias voltage.

For claim 6, Applicant requires the apparatus further comprises a power source of variable output against said cathode, wherein said control system also varies the cathode voltage by controlling the output of said cathode power source, said bias

Art Unit: 1753

sputtering film forming performed by controlling the output of said substrate power source based on said bias voltage functions.

Gopalraja discloses a sputtering process whereby a DC bias is supplied to the target and a DC bias is supplied to the substrate (col. 5, l. 2-6). The sputtering involves filling a substrate via (Figures 1 and 2). There are two phases to the sputtering. In the first phase, bias is supplied to the target and no bias is supplied to the substrate (col. 7, l. 34-42). In the second phase, the target bias is terminated (col. 8, l. 24-26) and a variable bias is applied to the substrate (Figure 6). In the first phase, more material is deposited on the sidewalls than on the bottom of the via (col. 7, l. 44-48) and thus, an irregularity is present. As can be seen From Figures 5 and 6, the bias to the substrate and target are varied. During the second phase, the sputtered particles are substantially vertical (col. 8, l. 26-44). The substrate bias and target bias are controlled by a controller (Figure 3). Gopalraja discloses the power source to be variable to the target and substrate (Figures 5 and 6) and to be controlled by a controller (Figure 3). As can be seen in Figure 6, the system continuously cycles through the different phases. Thus, the substrate is continuously varied because the phases are continuously cycled.

The difference between the present claims is that the substrate bias voltage corresponding to a stored value in a database stored in a control system is not discussed.

Shimamura et al. teach that a bias applied to a substrate can utilize a computer for controlling the biasing conditions. The computer stores substrate bias voltages in

Art Unit: 1753

data files. The data files are used selectively during the film forming process. (Column 10 lines 40-47) A method of applying a bias voltage to the substrate by using a radio frequency power is shown in Fig. 6. In Fig. 6 the first power applied to the substrate 102 is 200 W for a large voltage amplitude 601, and the second power applied to the substrate 102 is 10 W for a small voltage amplitude 602. The positive and negative voltage amplitudes of the first and second voltages with respect to zero volts are equal to each other. (Column 11 lines 47-60) During the film forming process, the biasing condition can be stabilized by detecting the substrate bias voltage and controlling the output of the radio frequency power supply 120 through a feedback circuit 151 to vary the level of the voltage waveform shown in Fig. 10 so that the substrate bias voltage will meet the data included in the file. (Column 12 lines 42-48) The object is to control the substrate bias so that the film has a uniform film thickness distribution. (Column 5 lines 40-48)

The motivation for utilizing a database for controlling the bias voltage is that it allows for forming a film with uniform thickness distribution. (Column 5 lines 40-48)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Gopalraja et al. by utilizing a database to control the bias voltage as taught by Shimamura et al. because it allows for forming a film with uniform thickness distribution.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gopalraja et al. in view of Shimamura et al. as applied to claims 1-3, 5 and 6 above, and further in view of Yamamoto (US 2002/0173144 A1).

For claim 4, Applicant requires the thin film to be used as a barrier layer or a seed layer for electrolytic plating.

Gopalraja is described above, but does not disclose what the deposited layer would be for. The disclosure is merely a teaching of how to adequately deposit a layer in a via of a substrate.

Yamamoto discloses that to when making a semiconductor integrated circuit, it is conventional to fill the recessed portion of the trench or via with a metal film such as copper by electrolytic plating after a copper seed layer is deposited by sputtering [0007]. When depositing the seed layer, it is conventionally to use a substrate bias to improve the substrate coverage [0012].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Gopalraja to deposit the layer in a via as a seed layer of copper and then fill it electrolytically because of the desire to form a semiconductor device.

### ***Response to Arguments***

Applicant's arguments filed 4-11-06 have been fully considered but they are not persuasive.

In response to the argument that Shimamura et al. fails to teach that the bias voltage corresponds to a stored substrate bias voltage value, it is argued that Shimamura et al. teach applying a bias voltage to a substrate to control deposition on a substrate. The bias voltage is controlled by a feed back circuit which controls the voltage of the substrate to meet data included in a data file. The data file includes

Art Unit: 1753

substrate bias voltages. The substrate bias voltage included in the data file is the stored substrate bias voltage as interpreted by the Examiner. Since the feed back controller controls the voltage of the substrate to meet (i.e. correspond to) the data in the file, the voltage of the substrate meets (i.e. correspond to) the voltage present in the data file. (See Shimamura et al. discussed above)

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rodney G. McDonald whose telephone number is 571-272-1340. The examiner can normally be reached on M- Th with Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam X. Nguyen can be reached on 571-272-1342. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.



Art Unit: 1753

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Rodney G. McDonald  
Primary Examiner  
Art Unit 1753

RM  
January 31, 2007